# Monday, 2nd July

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| 9h00-9h30 | Opening ceremony | |
| 9h30-9h50 | ANSOFT | |
| 9h50-10h10 | MARVELL | |
| 10h10-10h30 | INTERSIL | |
| 10h30-10h50 | Coffee break | |
| 10h50-11h10 | NXP | |
| 11h10-11h30 | NATIONAL SEMICONDUCTOR | |
| 11h30-11h50 | INFINEON | |
| 11h50-12h10 | INTEL | |
| 12h10-12h30 | STMicroelectronics | |
| 12h30-14h00 | Lunch Buffet at ENSEIRB (Main street) | |
| 14h00-14h40 | Invited: C.ENZ - EPFL, Switzerland | |
| | **Session Name: ADC I** | **Session Name: SOC I** |
| 14h50-15h10 | *Sharma Vivek*<br>Efficient pipelined ADCs using integer gain MDACs | *Figueiredo Monica*<br>Predicting Noise and Jitter in CMOS Inverters |
| 15h10-15h30 | *Volpi Emilio*<br>A non linear ADC for sensor linearization | *Rolland du Roscoat Laure*<br>Substrate Injection Characterization in CMOS Mixed Signal Systems on Chip |
| 15h30-15h50 | *Caldwell Trevor*<br>Time-Interleaved Incremental Data Converters with Low Oversampling Ratios | *L'Insalata Nicola Eugenio*<br>A Mesochronous Physical Link Architecture for Network-on-Chip Interconnects |
| 15h50-16h10 | *Hosseini Kaveh*<br>Calculation of Sequence Lengths in MASH 1-1-1 Digital Delta Sigma Modulators with a Constant Input | *Sahnine Chawki*<br>Efficient Design Approach and Advanced Architectures for Universal OFDM Systems |
| 16h10-16h30 | *Wu Rong*<br>A Fifth-order Continuous-Time Sigma-Delta Modulator with 62-dB Dynamic Range and 2MHz Bandwidth | *Nabi Syed Waqar*<br>A Dynamically Reconfigurable System-on-Chip for Implementing Wireless MACs |
| 16h30-16h50 | Coffee break | |
| | **Session Name: LNA** | **Session Name: MEMS** |
| 16h50-17h10 | *Zito Domenico*<br>1-V 13-GHz Ultra Low Noise Amplifier for System-on-a-Chip Radiometer in CMOS 90 nm | *Minoglou Kyriaki*<br>High density Integrated Optoelectronic Circuits for High Speed Photonic Microsystems |
| 17h10-17h30 | *Zito Domenico*<br>UWB 3.1-10.6 GHz CMOS LNA | *ElBarkouky Mohamed*<br>A low–power 6.3 GHz FBAR overtone–based oscillators in 90 nm CMOS technology |
| 17h30-17h50 | *Wang Wen-Chieh*<br>The 1-V 24-GHz Low-Voltage Low-Power Current-Mode Transmitter in 130-nm CMOS Technology | *Bordas Chloe*<br>High quality medium power RF-MEMS based impedance tuner for smart microsystem integration |
| 17h50-18h10 | *Cimino Mikael*<br>A RF circuit design methodology dedicated to critical applications | |
| 19h00 | Welcome Reception Château Castelterrefort | |

# Tuesday, 3rd July

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|---|---|---|
| 9h00-9h50 | Invited: F.Svelto - Univ. Pavia, Italy | |
| 10h00-10h20 | Coffee break | |
| | **Session Name: ADC II** | **Session Name: SOC II** |
| 10h20-10h40 | *Bonizzoni Edoardo*<br>Design of a Current Mode 6-bit 100 MS/s Flash A/D Converter with 0.75 pJ/conv-lev FoM | *Fons Mariano*<br>Embedded Security: New Trends in Personal Recognition Systems |
| 10h40-11h00 | *Mariano Andre*<br>High-Speed Multi-Bit Continuous-Time Bandpass Delta-Sigma Modulator | *DALMASSO Julien*<br>Systems-on-Chip: Use of Test Data Compression Technique to Reduce Test Time |
| 11h00-11h20 | Sanchez-Renedo Manuel<br>A Cascaded CT Sigma-Delta Modulator with NTF Zero and Simple Mismatch Tuning Method using Interstage Feedback | *Busonera Giovanni*<br>Optimizing the serialization factor in Networks-on-Chip: a case of study |
| 11h20-11h40 | *Bonizzoni Edoardo*<br>An Optimized Two Stages Low Power Sinc3 Filter for ΣΔ Modulators | *Boudabous Anis*<br>HW/SW FPGA Implementation of Vector Median Filter |
| 11h10-12h00 | *Stornelli Vincenzo*<br>A fully-differential Symmetrical OTA-based rail-to-rail Switched Buffer | |
| 12h00-14h00 | Lunch La Passerelle | |
| 14h00-14h40 | Invited: W. Sansen - KUL, Belgium | |
| | **Session Name: Sig Process** | **Session Name: Sensor ICs** |
| 14h50-15h10 | *Cobanoglu Ozgur*<br>A Full Custom Front-End ASIC Prototype "CMAD" for COMPASS-RICH-1 Particle Detector System | *Egambaram Thoppay Prakash*<br>An automatic pulse alignment method for slope controlled super-regenerative receiver systems |
| 15h10-15h30 | *Panhofer Harald*<br>A Current Measurement System for Automotive Application | *Jawed Syed Arsalan*<br>A Low-Power High Dynamic-Range Sigma-Delta Modulator for a Capacitive Microphone Sensor |
| 15h30-15h50 | *Dei Michele*<br>A Micro Power Capacitive Sensor Readout Channel Based on the Chopper Modulation Technique | *Aita Andre*<br>Low-Power and Accurate Operation of a CMOS Smart Temperature Sensor based on Bipolar Devices and Sigma-Delta A/D Converter |
| 15h50-16h10 | *Schipani Monica*<br>A low power CMOS interface circuit for three-axis integrated accelerometers | *Caboni Alessandra*<br>A integrated CMOS circuit for DNA hybridization detection with digital output and temperature control |
| 16h10-16h30 | *Rivet François*<br>A Software-Defined Radio based on Sampled Analog Signal Processing Dedicated to Digital Modulations | *Lazzerini Giovanni Mattia*<br>VHDL-AMS modeling of an integrated gas flow sensor readout channel with pressure compensation |
| 16h30-16h50 | Coffee break | |
| | **Session Name: PA** | **Session Name: IMAGE:VIDEO PROCESS** |
| 16h50-17h10 | *Tajalli Armin*<br>A Power-Efficient LVDS Driver Circuit in 0.18-µm CMOS Technology | *Ghio Alessandro*<br>A Support Vector Machine Based Pedestrian Recognition System on Resource–Limited Hardware Architectures |
| 17h10-17h30 | *Wernehag Johan*<br>Second Harmonic 60-GHz Power Amplifiers in 130-nm CMOS | *Sousa Leonel*<br>An ASIP Approach For Adaptive Motion Estimation On AVC |
| 17h30-17h50 | *Tapfuh Mouafo Joseph*<br>Low Level and High Linearity Amplifiers in integated technologies for satellite receivers: Technical issues of Linearization techniques | *Fons Francisco*<br>Flexible Hardware for Fingerprint Image Processing |
| 17h50-18h10 | *Luque Yohann*<br>A 0.13µm CMOS Push-Pull Cascode Power Amplifier for W-CDMA Application | |

# Wednesday, 4th July

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|---|---|---|
| 9h00-9h50 | Invited: F. Maloberti - Univ. Pavia, Italy | |
| 10h00-10h20 | Coffee break | |
| | **Session Name: Synhé/VCO** | **Session Name: SENSOR TECHNO** |
| 10h20-10h40 | *Zhipeng Ye*<br>Noise Reduction in Fractional-N Frequency Synthesizers with Multiphase VCO | *Durini Daniel*<br>Photodetector Structures for Standard CMOS Imaging Applications |
| 10h40-11h00 | *Del Re Stefano*<br>Low Voltage Integrated Astable Multivibrator Based on a Single CCII | *Kharrat Chady*<br>Microbeam dynamic shaping by closed-loop electrostatic actuation using modal control |
| 11h00-11h20 | *Tatinian William*<br>RTW VCO with Switched-Capacitor Tuning for Satellite Communication Applications | *Dahiya Ravinder S.*<br>Tactile Sensing Arrays for Humanoid Robots |
| 11h20-11h40 | *Majek Cedric*<br>The Factorial Delay Locked Loop: a solution to fulfill multistandard RF synthesizer requirements | *Battini Francesco*<br>Experiencing with AMR sensor conditioning in automotive field |
| 11h40-12h00 | *Zito Domenico*<br>UWB 3.1-10.6 GHz CMOS Transmitter for System-on-a-chip Nano-Power Pulse Radars | |
| 12h00-14h00 | Lunch La Passerelle | |
| 14h00 | Start to St Emillion | |
| | SOCIAL EVENT | |
| 20h00 | Gala Diner | |
| 23h30 | Back to Bordeaux | |

# Thursday, 5th July

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| 9h00-9h50 | Invited: P. Chevalier - STMicroelectronics, France | |
| 10h00-10h20 | Coffee break | |
| | **Session Name: Analog** | **Session Name: DIGITAL IC** |
| 10h20-10h40 | *Levi Timothée*<br>Scaling Guidelines for CMOS Linear Analog Design | *Pasquale Corsonello*<br>A New Noise-Tolerant Dynamic Logic Circuit Design |
| 10h40-11h00 | *Layton Kent*<br>Analog Circuit Design at and Below Vt+2Vds,sat | *Badel Stéphane*<br>Tri-State Buffer/Bus Driver Circuits in MOS Current-Mode Logic |
| 11h00-11h20 | *Mathew Mary*<br>Linear Differential Voltage-Current Converter | *Akgun Omer Can*<br>Design of Completion Detection Circuits for Self-timed Systems Operating in Subthreshold Regime |
| 11h20-11h40 | *Freitas Philippe*<br>Analog Circuits Design Base on Independently Driven Double Gate MOSfet | *Vincent Maingot*<br>On the Use of Error Correcting and Detecting Codes in Secured Circuits |
| 11h40-12h00 | *De Marcellis Andrea*<br>NIC-based Capacitance Multipliers for Low-Frequency Integrated Active Filter Applications | *Joye Neil*<br>Fault-Tolerant Logic Gates Using Neuromorphic CMOS Circuits |
| 12h00-12h20 | *Crombez Pieter*<br>A Linearity and Power Efficient Design Strategy for Architecture Optimization of gm-C Biquadratic Filters | *Stanisavljevic Milos*<br>Case Study of Fault-Tolerant Architectures for 90nm CMOS Crythographic Cores |
| 12h30-14h30 | Lunch La Passerelle | |
| | **Session Name: DSP** | **Session Name: CAD** |
| 14h30-14h50 | *Testoni Nicola*<br>Adaptive Wavelet-based signal dejittering | *Muhammad Waseem*<br>Separating Control and Data Processing in RT level Virtual IP Components |
| 14h50-15h10 | *Collard Bovy Anne*<br>A Ground Reflection Theory for UWB Transmission in the Case of CEPT Band Limited Spectrum | *Padovani Andrea*<br>Statistical Methodologies for Integrated Circuits Design |
| 15h10-15h30 | *Camino Pascal*<br>A Decimation Filter for a Very Large Band Signal in Radioastronomy | *Talay Selcuk*<br>Adaptive High Performance SDModulator Designs |
| 15h30-15h50 | *Mostardini Luca*<br>Advanced Digital Signal Inspector for internal signals of pin-limited systems on package | *Maehne Torsten*<br>Fostering the Reuse and Collaborative Development of Models in the AMS SoC Design Process |
| 16h00-16h30 | Closing Ceremony: Awards, Next year in Turkey | |